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PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE
(Honeywell Case No. H0005845-1600)
MBHB Case No. 04-031

In the Application of:

Mark D. Dvorak

Art Unit: TBD

Serial No.: 10/777,323

Examiner: To Be Assigned

Filed: February 12, 2004

For: Operational Amplifier with Selectable
Performance Characteristics

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

TRANSMITTAL LETTER

In regard to the above identified application:

1. We are transmitting herewith the attached papers for the above identified new patent application:

- ☒ Information Disclosure Statement;
- ☒ Information Disclosure Statement (IDS) PTO-1449 Form;
- ☒ Copies of IDS Citations (2 U.S. Patents, 2 Article Documents); and
- ☒ Return Receipt Postcard.

2. With respect to additional fees:

- ☒ No additional fee is required.

3. GENERAL AUTHORIZATION: Please charge any additional fees or credit overpayment to Deposit Account No. 13-2490. A duplicate copy of this sheet is enclosed.

4. CERTIFICATE OF MAILING UNDER 37 CFR § 1.10: The undersigned hereby certifies that this Transmittal Letter and the paper, as described in paragraph 1 hereinabove, are being deposited with the United States Postal Service as "First Class Mail", addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on this 17th day of May, 2004

Date: May 17, 2004

By: Joseph A. Herndon
Joseph A. Herndon
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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure provided by 35 C.F.R. § 1.56 and §§ 1.97-98, the applicant wishes to make the following reference of record in the above-identified application. A copy of the reference is enclosed. A copy is also listed in the PTO-1449 form enclosed herewith. It is requested that the document be given careful consideration and that it be cited of record in the prosecution history of the present application so that it will appear on the face of the patent issuing from the present application.

Portions of the reference may be material to the examination of the pending claims, however no such admission is intended. 37 C.F.R. 1.97 (h). The reference has not been reviewed in sufficient detail to make any other representation and, in particular, no representation is intended as to the relative importance of any portion of the reference.

This Statement is not a representation that the cited reference has effective dates early enough to be "prior art" within the meaning of 35 U.S.C. sections 102 or 103, nor submission to be construed as a representation that a search has been made.

CITED REFERENCES

U.S. Patents:

<u>No.</u>	<u>Issue Date</u>	<u>Author</u>
1. 2004/0008084	01/15/04	Mark D. Dvorak
2. 6,559,716	05/06/03	Sauerbrey et al.

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

3. IEEE 0018-9200/82/1200-0969 1982, "MOS Operational Amplifier Design – A Tutorial Overview", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 6, December 1982.
4. IEEE 0018-9200/94 1994, "Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages", IEEE Journal of Solid-State Circuits, Vol. 29, No. 8, August 1994.


Respectfully submitted,

McDonnell Boehnen Hulbert & Berghoff

Date: May 17, 2004

By: 

Joseph A. Herndon
Registration No. 50,469

Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office INFORMATION DISCLOSURE STATEMENT BY APPLICANT 	Honeywell Ref. No. H0005845-1600 MBHB Case No. 04-031	Serial No. 10/777,323
	Applicant: Mark D. Dvorak	
	Filing Date: February 12, 2004	Group: TBA

U.S. PATENT DOCUMENTS

Examiner Initial	No.	Document Number	Date	Name	Class	Subclass	Filing Date
	1	2004/0008284	01/15/04	Dvorak			
	2	6,559,716	05/06/03	Sauerbrey et al.			

FOREIGN PATENT DOCUMENTS

Examiner Initial	No.	Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS - Including Author, Title, Date, Pertinent Pages, Etc.

Examiner Initial	No.	Document
	3	IEEE 0018-9200/82/1200-0969 1982, "MOS Operational Amplifier Design – A Tutorial Overview", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 6, December 1982.
	4	IEEE 0018-9200/94 1994, "Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages", IEEE Journal of Solid-State Circuits, Vol. 29, No. 8, August 1994.

Examiner	Date Considered
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with any communication.